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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,839	03/25/2004	Stephen Strickland	EMC04-01(04011)	6718

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DAVID E. HUANG, ESQ.
BAINWOOD HUANG AND ASSOCIATES LLC
2 CONNECTOR ROAD
WESTBOROUGH, MA 01581

EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,839	STRICKLAND ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/6/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- **Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurio, U.S. Patent Number 5,774,640.**
- **Claims 21-24 are objected to as being dependent upon a rejected base claim**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurio, U.S. Patent Number 5,774,640.

3. Regarding claim 1:

a. Regarding the limitation of "in a data storage system having a first storage processor, a second storage processor and a communications subsystem coupled to the first and second storage processors, a method for operating the data storage system during a failure within the communications subsystem," Kurio discloses a system with a device drive connected to two network controllers for a communication system with storage device attached to the network controllers. (See the abstract, Lines 64-65 of Column 5 and Lines 1-17 of Column 6).

b. Regarding the limitation of "while the first and second storage processors perform data storage operations, enabling operation of the communications subsystem to provide communications between the first and second storage processors," Kurio

discloses a system a device drive that can communicate between the first and second controllers of the system. (Lines 40-47 of Column 2 and the abstract).

c. Regarding the limitation of "sensing a failure within a critical portion of the communications subsystem," Kurio discloses a system in which a failover to the second controller will occur upon detection of a failure in the first. (Lines 40-47 of Column 2 and the abstract)

d. Regarding the limitation of "resetting an interfacing portion of the communications subsystem in response to the sensed failure to enable one of the first and second storage processors to continue operation," Kurio discloses a system in which a reassignment of the first controller to the second controller happens upon detection of a failure (resetting an interfacing portion of the communication subsystem in response to the sensed failure) in the first by reassigning network and MAC address to the second controller from the first (to enable one of the first and second storage processors to continue to operation). (Lines 40-53 of Column 2).

4. Regarding claim 2, Kurio discloses a system that has a polling protocol for sending messages periodically to test the controllers for failure. Kurio also disclose that retransmissions of the polling request will occur until a maximum number of retires. (Lines 4-16 of Column 10).

5. Regarding claim 3, Kurio discloses a system that can switch the network traffic from a first controller to a second controller upon detection of a failure. (See the abstract). Kurio discloses a system in which a failover to the second controller happens upon detection of a failure in the first by reassigning network and MAC address to the second controller from the first. (Lines 40-53 of Column 2).

6. Regarding claim 4, Kurio discloses a system that can switch the network traffic from a first controller to a second controller upon detection of a failure. (See the abstract; also see Lines 35-48 of Column 8).

7. Regarding claim 5, Kurio discloses a system in which the device drive can detect that the controller of one of the computer system is in a DOWN state that can be cause by a lack of power to computer system. (Lines 7-10 of Column 14). Kurio also discloses hot-pluggable devices for adding and removing faulty device to the system. (A hot-pluggable device would result in the loss of an electrical connection). (Lines 25-37 of Column 5).

8. Regarding claim 6:

e. Regarding the limitation of "a first storage processor, a second storage processor, a communications subsystem having an interfacing portion interconnected between the first storage processor and the second storage processor, a clock circuit coupled to the interfacing portion, and a controller coupled to the interfacing portion and the clock circuit," Kurio discloses a system with a device drive connected to two network controllers for a communication system with storage device attached to the network controllers. (See the abstract, Lines 64-65 of Column 5 and Lines 1-17 of Column 6).

f. Regarding the limitation of "enable operation of the interfacing portion to provide communications between the first and second storage processors," Kurio discloses a system a device drive that can communicate between the first and second controllers of the system. (Lines 40-47 of Column 2 and the abstract).

g. Regarding the limitation of "sense a failure within the clock circuit," Kurio discloses a system in which a failover to the second controller will occur upon detection of a failure in the first. (Lines 40-47 of Column 2 and the abstract)

h. Regarding the limitation of "reset the interfacing portion in response to the sensed failure to enable one of the first and second storage processors to continue operation," Kurio discloses a system in which a reassignment of the first controller to the second controller happens upon detection of a failure (resetting an interfacing portion of the communication subsystem in response to the sensed failure) in the first by reassigning network and MAC address to the second controller from the first (to enable one of the first and second storage processors to continue to operation). (Lines 40-53 of Column 2).

9. Regarding claim 7, Kurio discloses a system that has a polling protocol for sending messages periodically to test the controllers for failure. Kurio also disclose that retransmissions of the polling request will occur until a maximum number of retires. (Lines 4-16 of Column 10). Kurio also discloses a watchdog timer. (Lines 29-35 of Column 12).

10. Regarding claim 8, Kurio discloses a system that can switch the network traffic from a first controller to a second controller upon detection of a failure. (See the abstract). Kurio discloses a system in which a failover to the second controller happens upon detection of a failure in the first by reassigning network and MAC address to the second controller from the first. (Lines 40-53 of Column 2).

11. Regarding claim 9, Kurio discloses a system where a device drive and two controllers are connected via a bus. (Lines 64-65 of Column 5 and Lines 1-17 of Column 6, also see Figure 3 items 311, 312, 111a,b and Figure 1, item 101).

12. Regarding claim 10, Kurio discloses a system with dual memory device being mirror and connected to the controllers and the device driver over the communication bus. (Lines 64-65 of Column 5 and Lines 1-17 of Column 6, also see Figure 3 items 311, 312, 111a,b and Figure 1, item 101).

13. Regarding claim 11, Kurio discloses a device driver couple to a first and second networked controller device. (see the abstract and Lines 7-24 of Column 5).

14. Regarding claim 12, Kurio discloses a system in which the device drive can detect that the controller of one of the computer system is in a DOWN state that can be cause by a lack of power to computer system. (Lines 7-10 of Column 14).

15. Regarding claim 13:

i. Regarding the limitation of "a first storage processor, a second storage processor, a communications subsystem having an interfacing portion interconnected between the first storage processor and the second storage processor, a clock circuit coupled to the interfacing portion, and a controller coupled to the interfacing portion and the clock circuit," Kurio discloses a system with a device drive connected to two network controllers for a communication system with storage device attached to the network controllers. (See the abstract, Lines 64-65 of Column 5 and Lines 1-17 of Column 6).

j. Regarding the limitation of "means for enabling operation of the interfacing portion to provide communications between the first and second storage processors," Kurio discloses a system a device drive that can communicate between the first and second controllers of the system. (Lines 40-47 of Column 2 and the abstract).

k. Regarding the limitation of "means for sensing a failure within the clock circuit," Kurio discloses a system in which a failover to the second controller will occur upon detection of a failure in the first. (Lines 40-47 of Column 2 and the abstract)

l. Regarding the limitation of "means for resetting the interfacing portion in response to the sensed failure to enable one of the first and second storage processors to continue operation," Kurio discloses a system in which a reassignment of the first controller to the second controller happens upon detection of a failure (resetting an

interfacing portion of the communication subsystem in response to the sensed failure) in the first by reassigning network and MAC address to the second controller from the first (to enable one of the first and second storage processors to continue to operation). (Lines 40-53 of Column 2).

16. Regarding claim 14:

m. Regarding the limitation of "communications subsystem for a data storage system having a first storage processor and a second storage processor; an interfacing portion configured to interconnect the first storage processor with the second storage processor; a clock circuit coupled to the interfacing portion; a controller coupled to the interfacing portion and the clock circuit," Kurio discloses a system with a device drive connected to two network controllers for a communication system with storage device attached to the network controllers. (See the abstract, Lines 64-65 of Column 5 and Lines 1-17 of Column 6).

n. Regarding the limitation of "enable operation of the interfacing portion to provide communications between the first and second storage processors," Kurio discloses a system a device drive that can communicate between the first and second controllers of the system. (Lines 40-47 of Column 2 and the abstract).

o. Regarding the limitation of "sense a failure within the clock circuit," Kurio discloses a system in which a failover to the second controller will occur upon detection of a failure in the first. (Lines 40-47 of Column 2 and the abstract)

p. Regarding the limitation of "reset the interfacing portion in response to the sensed failure to enable one of the first and second storage processors to continue operation," Kurio discloses a system in which a reassignment of the first controller to the second controller happens upon detection of a failure (resetting an interfacing portion of

the communication subsystem in response to the sensed failure) in the first by reassigning network and MAC address to the second controller from the first (to enable one of the first and second storage processors to continue to operation). (Lines 40-53 of Column 2).

17. Regarding claim 15, Kurio discloses a system that has a polling protocol for sending messages periodically to test the controllers for failure. Kurio also disclose that retransmissions of the polling request will occur until a maximum number of retires. (Lines 4-16 of Column 10). Kurio also discloses a watchdog timer. (Lines 29-35 of Column 12).

18. Regarding claim 16, Kurio discloses a system that can switch the network traffic from a first controller to a second controller upon detection of a failure. (See the abstract). Kurio discloses a system in which a failover to the second controller happens upon detection of a failure in the first by reassigning network and MAC address to the second controller from the first. (Lines 40-53 of Column 2, also see Lines 5-10 of Column 15).

19. Regarding claim 17, Kurio discloses a system where a device drive and two controllers are connected via a bus, which the examiner equates to a CMI bus. (Lines 64-65 of Column 5 and Lines 1-17 of Column 6, also see Figure 3 items 311, 312, 111a,b and Figure 1, item 101).

20. Regarding claim 18, Kurio discloses a system with dual memory device being mirror and connected to the controllers and the device driver over the communication bus. (Lines 64-65 of Column 5 and Lines 1-17 of Column 6, also see Figure 3 items 311, 312, 111a,b and Figure 1, item 101).

21. Regarding claim 19, Kurio discloses a device driver couple to a first and second networked controller device. (See the abstract and Lines 7-24 of Column 5, also see Lines 35-48 of Column 8).

22. Regarding claim 20, Kurio discloses a system in which the device drive can detect that the controller of one of the computer system is in a DOWN state that can be cause by a lack of power to computer system. (Lines 7-10 of Column 14).

Allowable Subject Matter

23. Claims 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

24. Applicant's arguments filed 01/04/2007 have been fully considered but they are not persuasive.

25. Regarding the arguments over claim 1 (pages 11-13 of the response):

q. At the request of the applicant (see page 12, end of 2nd paragraph, page 13 end of 1st, 2nd, and 3rd paragraphs), the examiner has added more detail to the rejection of claim 1-2 and 4-5 above; please refer to the more detailed rejection.

26. Regarding claim 2:

r. Regarding the applicant's argument over Kurio failing to teach a clock circuit (page 15 of the response), the examiner contends that the prior art does, in fact, disclose a clock circuit. Kurio discloses that polling protocol for sending messages is done periodically (Column 2, lines 55-58). The examiner contends that anything done periodically must have a time mechanism as a part of the device driver in order to accomplish the task periodically.

27. Regarding claim 4, please refer to the rejection for more detail.

28. Regarding claim 5, please refer to the rejection for more detail.

29. Regarding the arguments over claims 14-20 (pages 13-16 of the response):

s. At the request of the applicant (see page 15, end of 1st paragraph, page 16 end of 1st, 2nd, and 3rd paragraphs), the examiner has added more detail to the rejection of claim 14, 16-17 and 19 above; please refer to the more detailed rejection.

t. Regarding the applicant's argument over Kurio failing to teach a clock circuit (page 15 of the response), the examiner contends that the prior art does, in fact, disclose a clock circuit. Kurio discloses that polling protocol for sending messages is done periodically (Column 2, lines 55-58). The examiner contends that anything done periodically must have a time mechanism as a part of the device driver in order to accomplish the task periodically.

30. Regarding claim 16, Kurio disclose that an Ethernet controller can be reintegrated to the system and reassume the MAC address for the failover controller. The examiner contends this resetting of the configuration when the controller resumes its identity for the failover controller. (Lines 5-10 of Column 15).

31. Regarding claim 17, please refer to the rejection for more detail.

32. Regarding claim 19, please refer to the rejection for more detail.

33. Regarding the arguments for claims 6-13 (pages 16-17 of the response), please see the reply to arguments for claim 1 above.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

36. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

37. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

39. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

40. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

tmb
March 27, 2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER